

09/845,454

F0662/ AMDP662USAMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A system for monitoring and regulating an etch process, comprising:

at least one etching component that etches at least one portion of a wafer; an etch component driving system that drives the at least one etching component; a system that directs light onto one or more gratings located on at least one portion of the wafer;

an etch monitoring system that measures one or more etching parameters from light reflected from the one or more gratings; and

a processor operatively coupled to the etch monitoring system and the etch component driving system, the processor receives etching parameter data from the measuring system and analyzes the etching parameter data by comparing the etching parameter data to stored etching data to generate a feed-forward control data operative to control the at least one etching component, the processor further logically maps the wafer into one or more grid blocks and makes a determination of acceptability of etching values in the one or more grid blocks.

2. (Previously Presented) The system of claim 1, the etch monitoring system further comprises a scatterometry system that processes the light reflected from the one or more gratings.

3. (Previously Presented) The system of claim 2, the processor is operatively coupled to the scatterometry system, the processor analyzes data received from the scatterometry system and produces analyzed data, the processor controls, at least in part,

09/845,454**F0662/ AMDP662US**

the at least one etching component *via* the etching component driving system based, at least in part, on the analyzed data.

4. (Previously Presented) The system of claim 3, the etch process is at least one of descum etching, photoresist trim etching, breakthrough anti-reflective coating etching and main etching.

5. (Previously Presented) The system of claim 3, the etch process is at least one of an isotropic etch process and an anisotropic etch process.

6. (Previously Presented) The system of claim 3, the etch process is a dry-etching process where the mechanism of etching has at least one of a physical basis, a chemical basis and a combination of physical and chemical bases.

7. (Previously Presented) The system of claim 6, the dry-etching technique with a mechanism of etching as a physical basis is at least one of a glow-discharge sputtering technique and an ion-milling technique.

8. (Previously Presented) The system of claim 6, the dry-etching technique with a mechanism of etching as a chemical basis is a plasma etching technique.

9. (Previously Presented) The system of claim 8, the dry-etching technique with a combination of bases is at least one of a reactive ion etching (RIE) technique and an ion-enhanced etching technique.

10. (Cancelled).

11. (Previously Presented) The system of claim, the processor determines the existence of unacceptable etching values for at least a portion of the wafer based on comparing one or more measured etching values to one or more stored etching values.

09/845,454F0662/ AMDP662US

12. (Previously Presented) The system of claim 11, the processor employs a non-linear training system in computing feed-forward control data operable to adjust the at least one etching component.

13. (Currently Amended) A method for monitoring and regulating an etch process comprising:

logically partitioning a wafer into one or more portions;
etching the wafer with at least one etching component, where the at least one etching component is operable to etch at least one of the one or more portions;

driving the at least one etching component with an etch component driving system;

fabricating one or more gratings to be etched on the wafer;
directing an incident light onto at least one of the one or more gratings;
collecting a reflected light reflected from the one or more gratings;
measuring the reflected light with an etch monitoring system, where the etch monitoring system determines to determine one or more critical dimensions associated with the at least one grating;

receiving etching parameter data with a processor, where the processor is operatively coupled to the etch monitoring system and the etch component driving system;

computing one or more adjustments for one or more etching components with the processor, where the processor compares by comparing the one or more critical dimensions to scatterometry signatures associated with one or more stored critical dimensions; and

adjusting the etch process based, at least in part, on the one or more adjustments;
and

mapping the wafer into one or more grid blocks with the processor, where the processor makes a determination of acceptability of etching values in the one or more grid blocks.

09/845,454F0662/ AMDP662US

14. (Original) The method of claim 13, further comprising processing the reflected light in a scatterometry system.
15. (Original) The method of claim 14 wherein computing the one or more adjustments is based, at least in part, on data received from the scatterometry system.
16. (Original) The method of claim 15, wherein the etch process is regulated for portions of the wafer that have been etched.
17. (Original) The method of claim 15 wherein the etch process is regulated for unetched portions on the wafer that have not been etched.
18. (Original) The method of claim 15, wherein the etch process is regulated for subsequent wafers.
19. (Original) The system of claim 15, wherein the etch process is a dry-etching process where the mechanism of etching has at least one of a physical basis, a chemical basis and a combination of physical and chemical bases.
20. (Original) The system of claim 19, wherein the dry-etching technique with a mechanism of etching as a physical basis is at least one of a glow-discharge sputtering technique and an ion-milling technique.
21. (Original) The system of claim 19, wherein the dry-etching technique with a mechanism of etching as a chemical basis is a plasma etching technique.
22. (Original) The system of claim 19, wherein the dry-etching technique with a combination of bases is at least one of a reactive ion etching (RIE) technique and an ion-enhanced etching technique.

09/845,454F0662/ AMDP662US

23. (Currently Amended) A method for monitoring and regulating an etch process comprising:

logically partitioning a wafer into one or more grid blocks;

etching the wafer with one or more etching components, where the one or more etching components are operable to etch at least one of the one or more grid blocks;

driving the one or more etching components with an etch component driving system;

directing an incident light on at least one of the one or more grid blocks;

monitoring the etch process in at least one of the one or more grid blocks with an etch monitoring system, where the etch monitoring system analyzes by analyzing light reflected from the at least one of the one or more grid blocks; and

coordinating control of at least one of the one or more etching components with a processor, where the processor coordinates control based, at least in part, on the analysis of the light reflected from the at least one of the one or more grid blocks; and

mapping the wafer into one or more grid blocks with the processor, where the processor makes a determination of acceptability of etching values in the one or more grid blocks.

24. (Original) The method of claim 23, wherein the one or more grid blocks are measured at pre-determined intervals of time.

25. (Cancelled).

26. (Previously Presented) The system of claim 1, the one or more etching parameters relate to at least one of size of a feature on the wafer, shape of a feature on the wafer, location of a feature on the wafer, a chemical property of a wafer, size of gratings, shape of gratings, location of gratings, size of space between features, shape of space between features, and location of space between features.

27. (Currently Amended) A system that facilitates monitoring an etch process on a wafer, comprising:

09/845,454F0662/AMDP662US

means for etching at least one portion of a wafer;

means for utilizing an etch component driving system for driving the etching means;

means for directing light towards a grating resident upon the wafer;

means for measuring an etching parameter based at least in part upon light reflected from the grating;

means for utilizing a processor to logically partition the wafer into a plurality of grid blocks; and

means for storing accepted etching data in the processor; and

means for utilizing the processor to determine acceptability of a measured etching parameter within one of the plurality of grid blocks by comparing the etching parameter to the stored accepted etching data.